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SUMMARY OF RESEARCH "FINAL REPORT"

FINE COLLIMATOR GRIDS USING SILICON METERING STRUCTURE

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Foreword

The project Fine Collimator Grids Using Silicon Metering Structure was managed by Dr. Carol Eberhard of the Electromagnetic Systems & Technology Department (Space & Technology Division) of TRW who also wrote this final report. The KOH chemical etching of the silicon wafers was primarily done by Dr. Simon Prussin of the Electrical Engineering Department of UCLA at the laboratory on campus. Moshe Sergant of the Superconductor Electronics Technology Department (Electronics Systems & Technology Division) of TRW and Dr. Prussin were instrumental in developing the low temperature silicon etching processes. Moshe Sergant and George G. Pinneo of the Microelectronics Production Department (Electronics Systems & Technology Division) of TRW were instrumental in developing the processes for filling the slots etched in the silicon wafers with metal-filled materials. Their work was carried out in the laboratories at the Space Park facility. Moshe Sergant is also responsible for the impressive array of Scanning Electron Microscope images with which the various processes were monitored. Many others also contributed their time and expertise to the project. I wish to thank them all.

1.0 Summary

The High Energy Imaging Spectrometer (HEISPEC) images the sun in the X-ray wavelengths by using Rotating Modulation Collimators. HEISPEC requires the development of several technologies, such as the ability to fabricate X-ray collimator grids with very fine pitch and high accuracy. One design of an X-ray collimator grid consists of a regularly spaced series of slits cut into a slab of high-Z X-ray absorbing material, such as tungsten, tantalum, gold, or lead. A sketch of such a grid and explanations of grid terminology are shown in Figure 1.0-1. Photons pass through the slits but are strongly absorbed in the high-Z material areas. Identical pairs of these grids, when rotated in front of Ge and Si detectors, impose the spatial modulation necessary to reconstruct the X-ray emitting image at X-ray wavelengths. Typically tungsten has been the preferred material for both the grid frame and the slats.

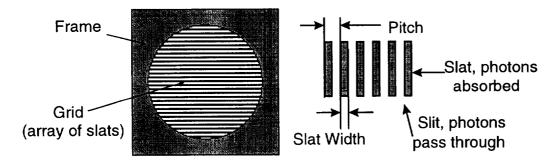


Figure 1.0-1. Schematic of X-ray Collimator Grid and Terminology

When the HEISPEC payload was sized for launch on the Pegasus XL launch vehicle, the collimator separation distance became 1.75 m to fit inside the Pegasus shroud. The collimator pitch requirements are driven by the collimator separation distance and range from 317 μ m down to 34 μ m in order to maintain the desired imaging resolution.

For the finest pitch grids, the pitch is $34 \, \mu m$, the slit width (photons pass through) is $20 \, \mu m$, and the slat width (photons are absorbed) is $14 \, \mu m$. To be effective, the array of slats must be very uniform, very straight and very parallel. The TRW approach to fabricating the finest pitch grids employs a hybrid collimator grid. Here the unwanted X-rays are absorbed by high-Z material slats held precisely in place by a metering structure composed of crystal silicon. This metering structure is chemically etched from a single monolithic silicon wafer. The silicon wafer must be very accurately cut so that the plane of the wafer is in the (110) configuration. The slots to hold the slats are aligned with the (111) plane of the crystal. This allows the etching process to remove the unwanted material along the weakest cleavage plane. The result of this is that the desired pattern which is imposed photolithographically on the surface of the wafer is maintained as the etching proceeds into the wafer.

Originally the slats were to be constructed from tungsten sheets nominally $12.5\,\mu m$ thick. Past experience with a $60\,\mu m$ pitch grid and tungsten slats $25\,\mu m$ thick indicated that the slats were very stiff and readily broke the $35\,\mu m$ thick metering structure walls which were supposed to

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hold them in place. Also, there was no source available which would assure us of providing 12.5 μm thick tungsten slats more than 3.75 cm long and the price was exorbitant. The decision was made to use slats made from gold ribbon of the appropriate thickness and width. This ribbon was available within a reasonable amount of time and for a reasonable price.

Acquiring the (110) silicon for the metering structure was more difficult. When the proposal was written, (110) silicon wafers were difficult, but not impossible, to obtain by means of special processing. The special processing consisted of cutting a cylindrical silicon boule grown in the [111] vertically to obtain rectangular wafers with (110) orientation. However, in the time between the proposal and the funding of the grant, the semiconductor industry demands changed. The silicon boule for special processing was no longer available, and the minimum time required became 3 to 4 years. We did, however, finally obtain 6-inch silicon wafers. The drawback was that the wafers were only 700 μ m thick, not the preferred 1500 μ m.

During this same time period, a mechanical engineering study of the original design indicated that this design would not be strong enough to survive the Pegasus XL launch vibration environment. The proposed bridge structure which supported most of the weight of the slats would break out, ruining the grid. These last two factors led us to a redesign of the fine grid metering structure.

The "platform" design is shown in Figure 1.0-2. The circular aperture is approximated by a regular hexagon. The hexagon is surrounded by a open area to allow the positioning of the slats in the etched slots in the "platform". The slats would still be $1170~\mu m$ in height, supported by slots 500 to $600~\mu m$ deep. A suitable space qualified adhesive would be applied around the perimeter of the hexagon as a last step to hold the slats in place. A circular hole in the center of the hexagon traversed by the slats would allow an area where there would be no absorption of soft X-rays by the silicon.

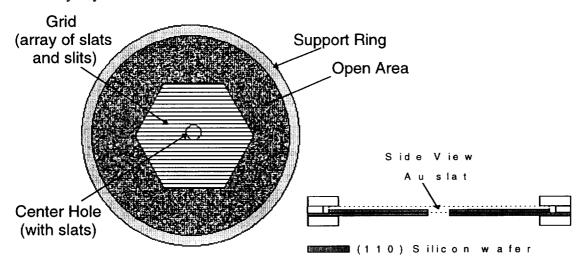


Figure 1.0-2. The Platform Design of the Silicon Metering Structure

With this design in mind, the required photomasks were constructed. A vendor was found to perform the photolithography which transferred the photomask pattern onto the wafers in lots of 4 wafers each. Chemical etching with KOH at 85 °C (as originally proposed) was initiated at UCLA, one wafer at a time.

As shown in Figure 1.0-3, the results were not good. The slots were uneven in depth and high aspect ratio etching was not being achieved as expected. The etching reaction is highly exothermic, generating heat and O_2 bubbles. The unevenness of the depth of the slots and the observed turbulence of the process led us to reason that the reaction was proceeding too fast and that the rates were locally uneven due to an uneven distribution of temperatures throughout the wafer. Also rapid bubble formation and bubble trapping in the very narrow slots would inhibit the free flow of the etchant required for high aspect ratio etching.

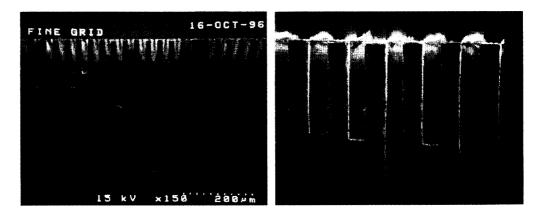


Figure 1.0-3. Scanning Electron Microscope (SEM) Image of Initial Etching Results

Successive lowering of the temperature of the etchant slowed down the reaction and led to better results, with the best results obtained at room temperature. Indeed, an aspect ratio near the theoretical limit was obtained.

 $D/U = (\text{slot depth})/(\text{undercut width on one side}) \sim 90$

Also the distribution of depths was much more uniform as shown in Figure 1.0-4.

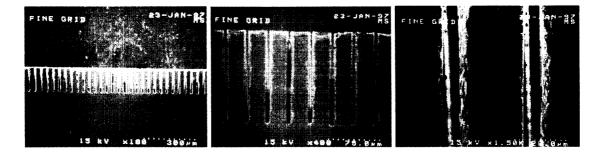


Figure 1.0-4. SEM Image of Low Temperature Etching Results

When a suitably etched portion of the hexagon pattern became available, it was submitted to the microassembly group to evaluate with respect to placing the gold ribbon into the slots. It was found that the 12.5 μ m gold ribbon was too soft and too thin to be placed reliably in the slots. The ribbon could be work hardened somewhat, but that would change its dimensions. This led to another redesign and an alternative method of producing the effect of a high-Z slat as shown in Figure 1.0-5. Uniform slots would be etched in the silicon wafers. The slots are filled with epoxy containing high-Z metallic (gold) powder. Although the X-ray absorption of the gold filled epoxy would not be as large as that of a solid gold slat, 2 or more wafers with identical patterns could be aligned to produce the same total cumulative absorption. Silver-filled epoxy was used for feasibility tests. Epoxy filled with very fine gold powder (5 μ m or less) is commercially available.

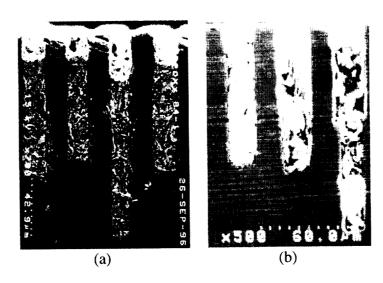


Figure 1.0-5. SEM Image of Slots Filled with (a) Ag-filled Epoxy and (b) Ag-filled Paint

One drawback here is that there is no way to place a hole in this structure to permit the passage of visible light and/or soft X-rays. On the other hand, the 1.15 nm line of the He-Ne laser is minimally absorbed by silicon and could be used for calibration and mapping the grid transmission. The spectrum of solar X-rays is very steep and the absorption of a large fraction of the soft X-ray spectrum by the silicon may still leave enough X-rays for imaging purposes.

We have demonstrated that under the right conditions, high aspect ratio etching, D/U ~ 90, is possible. An array of slots characterized by 15 μ m width, 34 μ m pitch and depths of ~ 500 μ m can be etched in the 700 μ m thick silicon wafers. We have also demonstrated that the technique of filling the slots with gold filled epoxy is possible. We have suggested a stacked design for the overall grid design and using the 1.15 μ m line of the He-Ne laser as an alternative method of calibration.

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2.0 Design Goals

The initial design goals are shown below in Figure 2.0-1. We proposed to demonstrate that a pair of fine pitch X-ray collimator grids with a circular aperture of 89.3 mm (3.5 inches) could be fabricated with tungsten slats to satisfy the requirements for the Pegasus XL launch vehicle.

GRID DIMENSIONS Circular aperture Shape: 89.3 mm Aperture: 1.17 mm Grid thickness: 34 µm Grid pitch: 14 µm Slat width: $20 \mu m$ Slit width: **GRID TOLERANCES** 3.4 µm Average pitch: .68 um Slit width: 3.4 µm RMS Position of each slat: 3.4 µm RMS Deviation of shadow edges: Flatness top and bottom edges: 200 µm RMS 200 µm RMS Grid thickness: +5, -0 mm Grid diameter: 1 μm Pitch matching, RMS slat displacement: MATERIAL Attenuation length for 500 keV X-rays < 5 mm Slat material: > 50% transmission for X-rays above 2 keV; Material between slats: < 10% obscuration of aperture for all X-rays **ENVIRONMENTAL** 0° C to +40° C Operating temperatures: Temperature difference between $< 10^{\circ} C$ front and back grid: per Pegasus XL User's Guide Launch loads:

Figure 2.0-1. Design Goals for Finest Collimating Grids

Severe environmental requirements must be met, primarily the launch loads. One grid of the pair was to be subjected to environmental testing to the levels identified with the Pegasus XL launch vehicle.

3.0 Components of the Grid

As discussed previously in section 1.0, the TRW approach to fabricating fine grids is a hybrid collimator grid, a variation of the slat placement technique. The grid design is driven by the need to maintain an array of long, parallel, straight, narrow high-Z material slats held precisely in place by a metering structure composed of crystal silicon. The slats are 12.5 µm thick, 1170 µm wide and range in length from approximately 45 mm to 90 mm. The unique aspect of this design is that the metering structure is chemically etched from a single monolithic silicon wafer using standard techniques developed by the semiconductor industry. Such structures can be made with an absolute dimensional accuracy of 1 µm or less. The only special requirement is that the silicon wafer must be cut in such a way that the plane of the wafer is in the (110) crystal configuration. This allows the etching process to remove the unwanted material along the weakest cleavage plane. The result is that the desired pattern, which is imposed photolithographically on the surface of the wafer, is maintained as the etching proceeds into the wafer. This fabrication concept is one of the fundamental techniques used in the field of micromachining and has been applied in a variety of ways to fabricate structures with sub-micron accuracy. The requirement that the high-Z material slat be rigidly supported by the metering structure implies the use of silicon wafers on the order of 2 mm thick. Based on the literature available at the time and the opinions of experts, the silicon wafers would be chemically etched with KOH at 45 % concentration at 85° C. We proposed to demonstrate that a pair of fine pitch X-ray collimator grids with a circular aperture of 89.3 mm (3.5 inches) could be fabricated with tungsten or gold slats to satisfy the requirements for the Pegasus XL launch vehicle.

3.1 Silicon Metering Structure

3.1.1 Technical Considerations in KOH Etching

The major issue is the etching of the high aspect ratio slots to the accuracy required for the metering structure. The entire surface of the silicon crystal wafer is initially protected from the etchant by a layer of silicon nitride which does not react with the etchant. Deep slots are etched in silicon by letting KOH etchant etch through a narrow slot made in the silicon nitride layer. The slot is made in the silicon nitride layer by the following standard photolithographic technique:

- 1. Apply photoresist uniformly to the nitride surface
- 2. Put the photomask holding the pattern to be transferred to the photoresist in place over the photoresist, adjusting the angular orientation as required
- 3. Expose the photoresist through the photomask
- 4. Develop the photoresist which removes the photoresist in the areas of the pattern, leaving the nitride layer unprotected by the photoresist
- 5. Plasma etch the surface of the wafer

The unprotected nitride layer is removed by the plasma etch, transferring the pattern from the photomask to openings in the nitride layer on the wafer. The remaining photoresist is cleaned from the wafer. Bare silicon, which reacts with the KOH etchant, remains in the pattern where the nitride has been removed.

The depth and width of the slot in the silicon is determined by etch rates in the two different directions as shown in Figure 3.1.1-1. The vertical direction is the [110] direction, and its etch rate is R[110]. The horizontal direction is designed to be the [111] direction, and its etch rate is R[111].

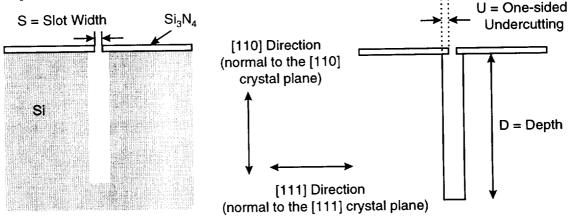


Figure 3.1.1-1. The Undercutting of the Silicon Nitride Layer during Etching of High Aspect Ratio Slots in Silicon

The ratio of the etch rates along the two crystal planes gives the final slot depth to slot width ratio, i.e.,

$$R[110]/R[111] = D/U,$$

where D is the desired slot depth and U is the undercut of the silicon nitride layer. If T is the desired total slot width, and S is the width of the slot opening in the silicon nitride coating, and U is the undercut to the silicon nitride, then

$$T = S + 2U$$
.

As the horizontal etching proceeds, the width of the slot grows and the silicon nitride layer is undercut. It has been established empirically that, as this undercutting proceeds, the walls of the slot remain vertical. Figure 3.1.1-2 shows the top of an etched slot with very high magnification. The opening in the silicon nitride layer can be seen.

The ratio D/U is a function of the deviation of the slot from true crystalline orientation. Actually, two components of the orientation are involved. One is the off-orientation of the wafer surface from the (110) plane and the other is the off-orientation of the mask pattern from the intercept of the (111) plane with the wafer surface.

Using X-ray diffraction patterns, the surface off-orientation with the (110) plane of each wafer can be measured. This should be in the range of 1 to 5 minutes. It is critical to align the slots parallel to the (111) cleavage plane. The (111) plane intersects the (110) plane at right angles.

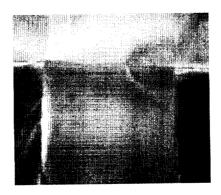


Figure 3.1.1-2. SEM Image of Slot and Opening in the Silicon Nitride Layer

Misalignment of the array of slots with the (111) plane results in a degradation of the D/U ratio, and since the etching proceeds by means of removing material parallel to the (111) plane, the walls of the slots exhibit a stair step effect if there is significant misalignment. To fine tune the alignment process, a fan pattern mask is used first.

The fan pattern mask pattern is opened up in the silicon nitride and etched while the rest of the wafer is still protected by the silicon nitride. The fan pattern consists of small portions of rays centered at the center of the mask. Each ray or spoke is a slot in the nitride 5 µm wide and is separated from the next ray or spoke by 3 arc minutes. The fan pattern is used to determine the correct orientation for the second mask with respect to the intersection of the (111) plane with the wafer surface. The fan pattern is etched until there is measurable undercutting for all the slots. The "best slot" is identified as the one with the least undercutting, centered in the minimum of the undercutting. This slot is used to align the second mask, or top mask, which contains the pattern of slots. The exact design and location of the fan pattern for this project was strongly influenced by the final design of the slat support structure in the silicon metering structure. Ideally the fan pattern should be outside the pattern of slots and slits or in an area which will be subsequently etched away entirely. Figure 3.1.1-3 shows a portion of the right half of the fan pattern.

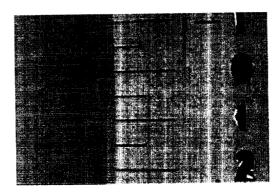


Figure 3.1.1-3. A Part of the Right Side Fan Pattern (Highly Magnified; Each ray is 5 μm wide.)

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The left side fan pattern is similar but reversed, with the negative angles at the bottom. The long lines mark the degrees from the zero line. The medium length lines mark the half degrees. There are 20 intervals per degree, so that there are 3 arc minutes between each of the shortest lines. After a preliminary etching, the etched slots are examined for undercutting. The minimum undercutting corresponds to the least off-orientation.

Figure 3.1.1-4 shows the observed one-sided undercutting as a function of angle. The line of intersection of the (111) plane with the wafer surface is +0.7°. When the orientation of the line of intersection of the (111) plane with the wafer surface is determined, the pattern defining the array of slots to be etched into the wafer surface can be aligned to minimize the slot off-orientation.

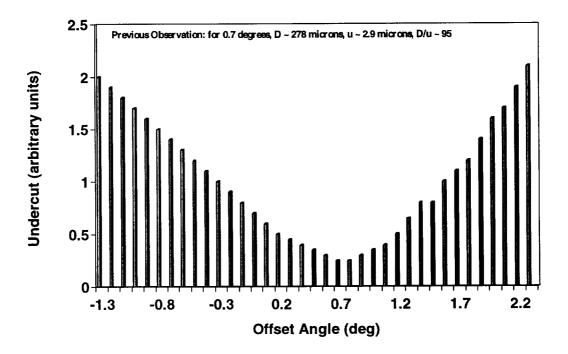


Figure 3.1.1-4. Observed One-sided Undercutting in the Fan Pattern as a Function of Offset Angle

When using very narrow slot openings, the etching process is difficult to control. This is because the narrow slot width in the mask has the effect of isolating the KOH in the slot from the general KOH solution resulting in the concentration of KOH in the slot decreasing as the etching proceeds, with a consequent changing of the etch ratio. The KOH depletion deep in the slot results in the etching becoming quite slow.

The original design layout for the proposed metering structure is shown in Figure 3.1.1-5. As can be seen, the rigid slats are secured on each end and supported in the middle by a silicon comb bridge. An issue arising from undercutting is that at the end of a narrow slot, other (111) surfaces develop so that for a distance of $\sqrt{3}$ D (where D is the slot depth) from the end of the

slot, the "floor" of the slot is not flat. This part of the slot cannot be used for holding a slat. Therefore, the total slot length is increased to compensate for this effect.

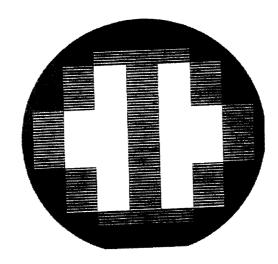


Figure 3.1.1-5. Original Design Layout for the Metering Structure Using Thick Silicon Wafers

Another effect also happens to the support combs which are intended to stabilize the slats. The edges lying in the (111) plane will be preserved. However, the edges lying perpendicular to this plane will be attacked. Thus the comb will be attacked and undercut to a distance equal to the slot depth on both exposed sides. The width of the support structure pattern must be increased to compensate for this effect. This last concern became irrelevant when it was determined that the original bridge structure design would probably not survive the launch environment.

3.1.2 Acquiring the Wafers

Ideally, the wafers would be fabricated and purchased with the proper orientations and those orientations verified. After the silicon wafers were lapped and polished to a thickness of 1500 μm , the edges would be rounded to reduce the potential for chipping and flaking along the edges. Then the wafers would be fully coated with silicon nitride.

In order to achieve the required aperture of 89.3 mm, a silicon wafer larger than 100 mm diameter must be used. Larger 6-inch boules are grown only by the major silicon producers, and they no longer grow any material in the [110] orientation. Semiconductor market demand supports only the [100] and [111] orientation boules in this size. In order to acquire wafers with the required orientation, special processing would be required. Starting with a 6-inch boule which is grown commercially in [111], a 5-inch slug would be cut from the boule. X-ray crystallography would be used to align the slug so that a flat may be cut parallel to the (110) plane. This results in a rectangular parallelepiped approximately 125 mm * 125 mm * 85 mm. The crystallographic axis must be verified using X-ray crystallography. From this piece, wafers would be cut with the proper (110) orientation. These wafers would then be lapped and polished down to a thickness of 2.0 mm. X-ray crystallography would be done on each wafer, which

would then be accurately lapped and polished to a lesser thickness with the (110) plane aligned within 5 minutes of the wafer surface.

Unfortunately, when the grant was initiated, the company which had offered special processing described above no longer had the required boule available. The (110) silicon wafers were unavailable through conventional means within a reasonable time frame. Additionally, Recticon, which had done the x-ray crystallography previously, was not making quotes on small projects. However, 25 6-inch wafers in the (110) orientation were finally obtained. The drawback was that each wafer was only 700 μ m thick. We began considering alternate designs.

3.2 High-Z Materials for Slats

In a previous effort, tungsten slat material proved to be extremely difficult to use. At the time, we performed numerous measurements on the sheets of tungsten foil received. The thickness requirements were met. Slats were chemically etched from the tungsten sheets. Although the material was of uniform thickness, long range variations in flatness (or undulations) over distances of 50 to 100 mm caused problems. Since tungsten was very stiff and was not sufficiently flat over the length of the slat, the slats were constantly breaking the thin walls of the slotted areas. For this reason, we looked at alternative slat materials. Also, there was no source available which would assure us of providing 12.5 μ m thick tungsten slats more than 3.75 cm long and the price was exorbitant.

The criteria for the slat material is that the attenuation length for 500 keV X-rays is less than 5 mm. The attenuation of X-ray and gamma-ray photons is exponential,

$$N(x) = N(0) \exp(-x/L)$$

where N(0) is the number of photons incident on the absorber, N(x) is the number that pass through a thickness of absorber, x, without interaction and L is the attenuation length. The absorption length is the figure of merit for the element, being the thickness of material needed to reduce the photon flux by a factor of (1/e) or 0.37. In terms of absorber properties,

$$L = (\rho \sigma)^{-1}$$

where ρ is the mass density and σ is the mass attenuation coefficient. For gold, the photon attenuation length at 500 keV is 3.43 mm, well below the 5 mm requirement.

Rhenium was also considered as potential slat material, but at the time only one company was known to work with rhenium. Discussions indicated that there was little current experience with producing foil or ribbons with the thicknesses and tolerances required for this project.

The decision was made to fabricate the high-Z slats from gold ribbon of the appropriate thickness and width. This ribbon was available within a reasonable amount of time and for a reasonable price. The 99.99% gold ribbon, (0.00055 ± 0.00005) inches thick by (0.046 + 10%) inches wide was ordered from Sigmund Cohn Corp. The thickness of the ribbon was a critical parameter

because it determined the clearance between the slats and the holding slots. The individual slats would be cut from the ribbon using standard techniques to minimize burrs on the edges or deformations caused by cutting. Several different lengths would be used to cover the aperture. The slats would be individually inserted into the silicon metering structure. Existing equipment for fine scale assembly work would be used to assemble the grids. Although experimentation would be required to discover the best methods for assembly of the ribbon slats into the etched slots, we were assured that such tolerances were not unusual in the microassembly area of expertise.

4.0 Design

Throughout this effort, the wafer design was driven by the requirements for the finest grids and the materials available for their fabrication using the proposed methods.

4.1 Original and Stacked Design

The original design involved rigid slats fixed into thick silicon wafers. Chemical etching of the silicon would be done with 45 % KOH at 85 °C to maximize the high aspect ratio etching. The original design of the silicon metering structure is shown in Figure 3.1.1-4. When it was learned that the thick wafers (1.5 mm) would not be available, we began considering alternate designs involving stacking and matching two etched wafers of the (110) orientation to form the metering structure. A supporting silicon structure for the etched wafers could be constructed from silicon in other orientations which was both plentiful and cheap. Figure 4.1-1 shows one such stacked design.

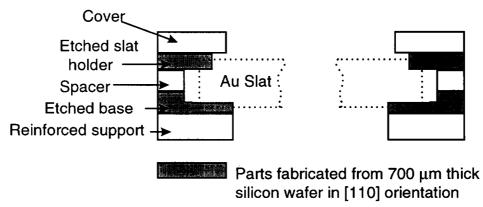


Figure 4.1-1. Stacked Design Layout for the Metering Structure Using Thin Silicon Wafers (Bridge not Shown)

At the same time that the stacked design was being studied, a mechanical engineering study was examining the original grid design with respect to surviving the Pegasus XL launch vibration requirements. The silicon bridge which was present in both the original design and in the stacked design supported most of the weight of the high-Z metallic slats. It was concluded that the original bridge design would break out during launch vibration, ruining the grid. The bridge in the stacked design would be even thinner and less durable.

4.2 Platform Design

The platform design was developed as an alternative to those designs featuring bridges. This design is shown in Figure 1.0-2. This design still utilized rigid slats supported by slots etched into the silicon wafer. The area around the slats was left open (the silicon nitride removed totally) and the open area would etch even more deeply than the slots by a ratio of at least 10/7. This would provide access to the edges of the raised platform to allow the insertion of slats. A more detailed cross section sketch of the platform design is shown in Figure 4.2-1. The platform design featured a center hole traversed by the gold slats through which low energy photons could pass without absorption. Around the outside of the platform, the edges would be supported by ordinary silicon support ring.

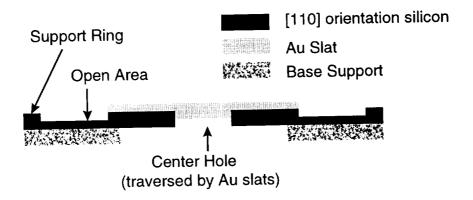


Figure 4.2-1. Cross Section of the Platform Design Metering Structure (Not to Scale)

The requirements on the material between the slats are as follows:

- > 50% transmission for X-rays above 2 keV
- < 10% obscuration of aperture for all X-rays

Since silicon is a low-Z material, its cross-section to X-rays is much lower than that of gold in the higher energy range of interest, so the auxiliary silicon support structure for the slats could be placed directly over the aperture of the grids with little loss of throughput. Most photons with energies below 10 keV would not be transmitted through the 1.4 mm of silicon in the platform. However, between 5 and 10 keV, transmission begins and for energies above 10 keV there is little attenuation. The 1 cm diameter hole traversed by the gold slats in the center of the wafer would allow the transmission of low energy photons without absorption. The X-ray spectrum rises very steeply for lower energies, so even very extensive obscuration by silicon would only serve to flatten the observed spectrum, and if properly calibrated, would not degrade the data.

Based on this design, two photomasks were ordered:

The "fan pattern mask" which located the fan pattern in the open area, aligned with the expected alignment of the intersection of the (111) and (110) crystal planes

The "top mask" defining the array of slots with the center hole, the open areas and top support ring

Twelve of the wafers were sent to have the center hole cut by means of laser machining. Then all of the wafers were sent to International Wafer Service, or IWS, for coating with 2500 Angstroms of silicon nitride and initial placement of the fan pattern on the wafers. IWS was successful in coating the wafers with nitride but was unable to manage the initial placement of the fan pattern on the wafers with the center hole. At that point we turned to a local contractor, Thin Film Devices or TFD, with extensive experience in micron scaled photolithography on large planar areas. Wafers were sent to TFD in lots of four for fan pattern placement. Chemical etching would be done at the UCLA Electrical Engineering Microelectronics Laboratory under the supervision of Dr. Simon A. Prussin.

There were difficulties from the beginning. The wafers were etched in 45 % KOH solution at a temperature of 85 °C for only a few hours. In spite of TFD's experience, the nitride in the fan patterns was not always opened up on both sides of the wafer. In some cases only one side of the fan pattern would etch. We were able to define the spoke with the minimum undercutting from examining only one pattern. After the first lot of 4 wafers with the incompletely etched fan patterns, we instructed TFD to increase the plasma etching time by 20 % (corresponding to 3000 Angstroms of nitride) to insure that the nitride layer would be removed. The nitride on these wafers seemed extremely vulnerable to scratching, much more so than in previous efforts. After etching and examining the fan patterns on the first two lots of four wafers, we chose the best four wafers and sent them to TFD for placement of the top mask pattern on the nitride.

Each step in the etching sequence must be performed exactly, but probably the most crucial step in achieving high aspect ratio etching occurs when the top mask pattern is transferred to the nitride. The top mask defines the slots that hold the slats. The slots in this mask are narrower than the width of the desired slots in the silicon wafer to allow for the undercutting which will occur. The top mask contains two very narrow black lines whose placement must be matched exactly to the spoke of the fan pattern with the least undercutting, one line at each fan pattern. Figure 3.1.1-2 shows a portion of the right side fan pattern. When the two alignment marks are aligned with the spoke of the fan pattern with the least undercutting, the array of slots (Figure 1.0-2) on the platform is also aligned to achieve the least amount of undercutting. The spoke number corresponding to the least amount of undercutting was consistently in the range from + 12 to + 14, or +0.6° to +0.7° from the 0° spoke of the fan. The top mask also contains large open areas. It is important to note at this point that the open areas have been observed to etch faster than deep slots.

TFD transferred the top mask pattern to the nitride and returned the wafers for etching. The slots were to be etched down to a depth which would restrain the slats. The wafers were etched one at a time in 45 % KOH at 85 °C as planned. The initial results were disturbing. After the wafer had been etched until the width of the slot was about 15 μ m, the wafer was sectioned and

scanning electron microscope pictures were made of the cross section of the array of slots. Figures 1.0-3 and 4.2-2 show results from these experiments.

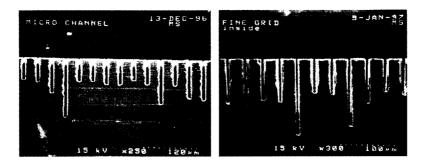


Figure 4.2-2. SEM Image of the Ragged Distribution of Slot Depths

The observed D/U ratio was only on the order of 14.6, much less than expected, and the distribution of depths was not at all uniform. Previously, we had etched a 60 μ m pitch pattern using a top mask in which the openings were 10 μ m, and the D/U ratio was approximately 67. We cut the next wafer into several segments and began experimenting with varying etching configurations, for example, slots up versus slots down.

Simon Prussin consulted with Don Kendall (the original researcher of high aspect ratio etching) about potential causes for this unexpected outcome. Although Kendall pointed out that there were various factors which might cause problems, he did not feel that any of these were compelling. Among these factors were the following:

- 1. The wafers were not oxidized prior to the application of silicon nitride. This process involves raising the temperature to 1050-1100 °C for a period of time before returning the temperature to normal. Then the silicon nitride layer is then deposited around 700-800 °C. The layer of oxide particles forms an amorphous, glass-like coating which seems to affect etching. Thick silicon nitride deposition can cause high stress within the nitride layer. This stress can be transferred to the silicon by strong surface contact. An oxide layer reduces stress.
- 2. Kendall also suggested that maybe the silicon nitride in the pattern area of slots was not really cleaned out by the plasma etching. Plasma etching of the fan patterns had been a problem in the past.
- 3. Kendall also discussed possible contamination of the etching solution. We were using premixed etching solution and the impurities were in the parts/million. We were also using great care to avoid accidental contamination. We felt that this was not the problem.

Kendall also pointed out that other wafers cut from this particular boule were well known to various experimenters and processors and had not presented any difficulties in the past.

We sent one representative wafer to Semiconductor Processing Company in Boston, MA, for X-ray crystallography measurements of the orientation of the top surface and the primary flat. The surface plane of the wafer was measured to be the (110) orientation within the measurement tolerances of their equipment (\pm 0.2°). Using the Avant computer assisted design equipment, the placement of the fan pattern on the wafers was verified to be accurate, with the maximum

15

observed deviation of 0.28°, well within the adjustment range of the fan pattern which covered from +2.5° to -2.5° in steps of 0.05°. Neither the wafers themselves nor the positioning of the fan patterns were the source of significant misorientation.

We began to think about the reaction kinetics of the etching. The KOH reaction with crystal silicon is highly exothermic. The reaction products include soluble silicates and O_2 gas bubbles. The soluble silicates could sink to the bottom of the slot, inhibiting the circulation of the fresh KOH solution. The results would be that the KOH would become depleted in the bottom of the slot. The opening of the slot in the silicon nitride is only 4 μ m wide. It would be very possible for the O_2 bubbles to build up below the opening in the nitride, further inhibiting the circulation of the fresh reactant. Possibly the observed deeper slots were those in which circulation was freer and unobstructed, for whatever reason.

In this same time period, a seminar was given at UCLA by Dr. Kenneth Breuer of MIT on "Gaseous Flows in Micron-Sized Geometries". The mechanics of flows in micron-sized structures are not completely understood. The Navier-Stokes equations may even be an inadequate representation of the fluid's behavior due to molecular effects. The difficulties with the usual flow equations in micron-sized geometries were discussed. Therefore, it is not unreasonable to assume that etchant flow in the slots would also be adversely affected by geometries on the order of a few microns.

We reasoned that the exothermic reaction could cause uneven temperature distributions leading to uneven reaction rates, uneven bubble formation leading to local buildups, and uneven turbulence in the slots. The first change we made was to reduce the etching temperature from 85 °C to room temperature, about 20 °C, in several steps. Since the top photomask was already made, there was little we could do about the 4 μ m openings in the nitride.

These changes brought a striking improvement to the results. Some of the results from the first cold etch interval are shown in Figure 1.0-4. The depths of the slots were very uniform at 140 μm . Depending on the magnification (X1500 or X3000) of the SEM image measured, the average total width was 6.15 μm or 7.1 μm . For an opening in the nitride of 4 μm , the one-sided undercutting is ~1.1 μm or ~1.6 μm . Thus the D/U ratio would be either 127 or 87.5. The depth etching rate, $R_{[110]}$ ~0.75 μm /hour. Indeed, this led to the problem that if the D/U ratio is 127, achieving a total width of 15 μm would lead to D ~ 700 μm , etching through the wafer. The wafer segment was returned to etching solution for a second interval.

After etching for the second interval, the average depth was 278 μ m, with a standard deviation of 22 μ m. Some of the results obtained after the second cold etch interval are shown in Figure 4.2-3. The distribution of depths was less uniform. Again the measured width depended on the magnification of the SEM image measured. The undercutting ranged from ~2.71 μ m to ~3.2 μ m, yielding D/U ratios from 103 to 87. The design goal would be D/U ~ 90 to 100.

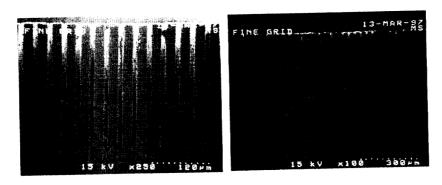


Figure 4.2-3. SEM Image of Slots after Second Cold Etch Interval

A segment of an etched wafer and some of the gold ribbon were given to personnel in the microassembly group for evaluation. There were two questions:

- 1. Was the slot opening sufficient to place the slat in the slot?
- 2. Was the gold ribbon stiff enough to be placed within the slot?

The average width of the slots in the test segment was $16.6\,\mu m$. The number of slats to be placed in each grid metering structure (~2600) caused concern about the time required for this task. Nevertheless, at the beginning of the evaluation the microassembly personnel were optimistic that this was feasible. Based on the evaluation, the characteristics of the gold ribbon may be summarized as follows:

Stiffness: The ribbon has some inherent stiffness; it's not limp. A short piece can be held in a tweezers and the ribbon will project outward, horizontally from the tweezer-gripped area. If the ribbon is moved very fast, however, its mass would bend the projected ribbon at the tweezers.

If the ribbon could be placed in a slot so that the lower 1/3 was supported in the slot, could it hold up its own weight? Yes, if you could get a portion of it into the slot, it would support its own weight, as in above.

How could the ribbon be inserted into the slot? The best method would be to slide it into the slot from above, edgewise. At some slot-width, this should be feasible at some low speed, limited by manual skill. A uv-curable adhesive could be used to bond it at one end of the trench, once one end was inserted. Hot-melts and other non-space rated materials also could be used to rapidly tack the ribbon in place. If one end is inserted into a slot, pulling and aligning the other end of the ribbon would not contribute to keeping the starting end in the slot. The ribbon probably would not be stiff enough to slide down the slot.

Is there some kind of y device which could assist in inserting the gold ribbon into the slot? Initially, a mechanical device like a large tweezers with means to grab a length of ribbon and stretch it and then keep the ribbon in tension was considered. This type of "tensioner" might be used to make straight-enough lengths of ribbon that they could be engaged on one end with the slot and then released and gently nudged into alignment with the rest of the slot. It would be necessary to immediately bond the ribbon in place at both ends so neither end could bounce up out of the slot.

In spite of the optimistic evaluation above, the results of the experiment to place the gold ribbon slats into the slots of the test segment with were not good. Independent of the depth of the slot,

the 16.6 μm width of the slot was not sufficiently wide to insert the 12.5 μm thick gold ribbon and the gold ribbon was too soft to force into the slot.

An alternative method for filling the slots with high-Z material was suggested by George Pinneo of the Microassembly Group. This method consists of filling the slots etched into the silicon with gold-filled epoxy. If the epoxy contained large particles, voids in the filling could develop. The particle size in the standard gold-filled epoxy in on the order of 15-20 µm. However, Epo-Tek would compound one in which the particle size is 5-10 µm. It would be expected to be very viscous, but warming the epoxy paste should decrease the viscosity and encourage metal-settling. Vibration and/or pressurizing might help increase the groove-fill. Slots could be filled and cured repeatedly until totally filled. As a feasibility test, some off-the-shelf silver-filled epoxy was used to fill the slots on one of the wafer test segments. The results of this test are shown in Figure 1.0-5. Another approach would be to use very fine powder of gold-tin solder. The slots would be filled with the fine powder which melts at a relatively low temperature. The process of filling and melting could be repeated until the slot was filled. Silver paint was also tried with some success.

When using 700 μ m thick wafers, the slots should be no more than 500-600 μ m deep. Since the density of gold in the epoxy filling would be less than that of a solid gold slat, it would be necessary to fill the slots on three wafers, align them exactly and bond them together for a stacked design.

4.3 Final Projected Grid Design

The final projected design for the silicon metering structure does not involve any open areas or holes. The aperture is circular and the slots are etched into the surface of the (110) plane of the silicon wafer. This design is shown in Figure 4.3-1.

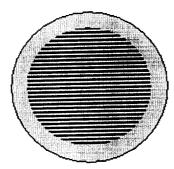


Figure 4.3-1. Top View of the Final Projected Grid Design (Fan Patterns and Wafer Flats Not Shown)

After chemical etching of the slots, the slots are filled with Au-filled epoxy. The process of filling with epoxy and curing is repeated until the slots are full. Three structures are aligned optically using an infrared alignment device and the stack is bonded together. Although the loss of the center hole would prevent the transmission of photons below about 8 keV, good transmission would be obtained for the higher energy photons.

It is possible to use the 1.15 μ m line of the He-Ne laser system to map the transmission function of the grids. The extinction coefficient k at that wavelength has been measured to be 5.8 x 10^{-6} (<u>Handbook of Optical Constants of Solids</u>, edited by Edward D. Palik, Academic Press, Inc.). The extinction coefficient k is related to the absorption coefficient α through

$$k = (4\pi/\lambda) \alpha$$
.

The intensity of a beam of photons as it propagates through a medium is exponential,

$$N(x) = N(0) \exp(-x/L) = N(0) \exp(-\alpha x)$$

where N(0) is the number of photons incident on the medium, N(x) is the number that pass through a thickness of medium, x, without interaction and L is the attenuation length. Therefore,

$$\alpha = (1/L)$$
.

A photon of wavelength $\lambda = 1.15~\mu m$ has 1.08 eV of energy. From the measured value of k for this photon energy, the attenuation length, L, is 15.8 mm, much larger than any accumulated path length in silicon when either four 0.7 mm thick wafers are stacked in one grid or eight wafers are taken together in the pair of grids. For this reason, the 1.15 μm line of the He-Ne laser system should be ideal for mapping the transmission functions.

5.0 Conclusions

Throughout this three-year effort, the objectives have remained the same: to research the construction of a 34 μ m pitch collimating grid with a silicon metering structure and high-Z metallic slats, making use of the anisotropic etching properties of crystalline silicon and the high absolute positioning accuracy developed by the semiconductor industry. Working with crystalline silicon has several advantages in producing objects with micron-sized features:

- 1. When the silicon wafer is very accurately cut so that the plane of the wafer is in the (110) configuration, and the slots to hold the slats are aligned closely with the (111) plane of the crystal, the etching process removes the unwanted material along the weakest cleavage plane, so that the array of parallel slots is maintained as the etching proceeds into the wafer from the surface. The slots etch perpendicularly into the wafer as the etchant attacks the surface of the (110) plane.
- 2. The smoothness of the slot walls is controlled by the alignment of the array with the intersection of the (111) plane with the (110) plane. If the slots are aligned closely parallel to the (111) plane, smooth and parallel slot walls develop as the etching proceeds. If the slots are not closely aligned, the walls while remaining roughly parallel develop in a stair step pattern which approximates the imposed pattern, but these walls are not smooth.

- 3. The depth-to-width ratio of the slot is also controlled by the alignment of the array with the intersection of the (111) plane with the (110) plane.
- 4. The width of the slots is controlled by frequent inspection during the etching process.
- 5. The pitch of the array of slots, which is imposed by the photomask, is accurate to less than $1 \mu m$.

Although we initially suffered problems in controlling the reaction kinetics, we were successful in defining a process for etching an array of high aspect ratio slots into the surface of the (110) plane of the silicon wafer. Assuming a total slot width of 15 μ m and a conservative (D/U) ratio of 80, slots 400 μ m deep can be etched in each 700 μ m thick wafer. Depending on the density of the high-Z material in the slot, three or four wafers could be aligned and stacked to form a single grid, providing the required X-ray absorption. The total thickness of such a stack would be 2.1 or 2.8 mm.

We have successfully defined and demonstrated processes for filling the slots with metal-filled epoxy and metal-filled paint. Silver was used in the test cases, but gold fill-material is available. Although more research is needed to determine the gold density of the epoxy in the slots, we have suggested a stacked design of either three or four wafers for each grid. The alignment of the stack could be done optically using an infrared alignment device. The transmission function of the grid can be mapped using the 1.15 µm line of the He-Ne laser system.

A patent application has been filed for the process of filling the silicon metering structure with a high-Z metal-filled compound, and another patent application is pending for the process of low temperature silicon etching to construct a fine collimating grid with a silicon metering structure.